ABSTRACT OF THE DISCLOSURE

A carrier lock detector for a QPSK or 4-QAM system implements a lock detection algorithm that maps detected signals onto one of first and second areas associated with nominal states defined by $(I_2 \oplus I_3)\cdot(Q_2 \oplus Q_3)$ and $\overline{Q_1 \oplus Q_2}\cdot\left(I_1\overline{I_2}\,\overline{I_3}+\overline{I_1}I_2I_3\right)+\left(\overline{I_1 \oplus I_2}\right)\cdot\left(Q_1\overline{Q_2}\,\overline{Q_3}+\overline{Q_1}Q_2Q_3\right)$, or alternatively, by $\left(\overline{I_1 \oplus I_2}\cdot\overline{Q_2 \oplus Q_3}\right)+\left(\overline{Q_1 \oplus Q_2}\cdot\overline{I_2 \oplus I_3}\right)$, respectively. When detected signals map onto one of the first areas, a first signal is generated. When detected signals map onto one of the second areas, a second signal is generated. When a difference between the first and second signals exceeds a threshold, a carrier lock detection signal is generated to enable a decoder. The carrier lock detector is able to detect carrier lock at a raw BER of 1e-2 or greater at a very low signal-to-noise ratio.